3. (Once Amended) A method for forming a via hole of a semiconductor device according to claim 2, wherein said annealing process for said via hole is performed at a low oxygen partial pressure.

REMARKS

Claim 2 was rejected under 35 U.S.C. §112, second paragraph, as lacking proper antecedent basis. Claim 2 has been rewritten to overcome this rejection.

Claim 2 was rejected under 35 U.S.C. §102(b) as being anticipated by Donnelly, Jr. et al., U.S. Patent No. 6,143,658. Claims 3-5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Donnelly, Jr. et al., in view of Tsuchiya et al., Digest of Technical Papers, Symposium on VLSI Technology (1997), pp. 59-60, and Hung et al., U.S. 2001/0008226 A1. Claims 6-9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Donnelly, Jr. et al., in view of Tsuchiya et al., and Hung et al., and further in view of Activac Technology Inc. Auto 306 Data Sheet. Finally, claims 10 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Donnelly, Jr. et al., in view of Tsuchiya et al., Hung et al., and Activac Technology Inc. Auto 306 Data Sheet, and further in view of Takagi et al., U.S. Patent No. 6,174,796 B1.

Donnelly et al. apparently fails to show or suggest an important technical feature of the present invention in which an annealing process should be performed before the step of sputtering for making a barrier film on a surface of the via hole is performed. Accordingly, the applicant believes that the present invention as defined by amended claim 2 would not be anticipated by Donnelly et al. and thus the anticipation rejection of claim 2, under 35 USC §102(b), should be withdrawn.

Regarding the present claims 3 to 5, although the Examiner rejected claims 3 to 5 under 35 USC §103(a) as being obvious to a person skilled in the art over Donnelly et al. in view of Tsuchiya et al. and Hung et al., none of these cited references shows or suggests the above-mentioned technical feature of the present invention.

Specifically, Donnelly et al. and Tsuchiya et al. never show or suggest performing an annealing process just before the sputtering operation is carried out. Moreover, although the Examiner apparently decided that there must be no substantial difference between the annealing process of the present invention and the oxygen plasma treatment as used in Hung et al., since Hung et al. discloses using oxygen plasma treatment in the via hole forming process, the oxygen plasma treatment of Hung et al. is used for removing organic material such as, for example, photoresist or the like from a surface of a substrate.

More precisely, in Hung et al., the oxygen plasma treatment is used for oxidizing copper (Cu) existing on a surface of a substrate ($Cu \rightarrow CuO, Cu_2O$) and this results in degradation of electrical conductivity at a connecting portion formed by Cu. On the other hand, in the present invention, the annealing process has a function of reduction, that oxide(s) of copper, (CuO,Cu_2O), formed on a surface of Cu is reduced to Cu ($CuO,Cu_2O \rightarrow Cu$), thereby improving the electrical conductivity of the connecting portion formed by Cu.

Thus, the annealing process of the present invention serves a completely adverse chemical function to the oxygen plasma treatment as shown in Hung et al. In other words, both treatments are opposite treatments from each other.

Regarding claims 6 to 11, although the Examiner rejected those claims under 35 USC §103(a) as being obvious to a person skilled in the art over Donnelly et al., in view of Tsuchiya et al. and Hung et al. as well as Active Technology Inc. Auto 306 Data Sheet, and further in view

of Takagi et al. for claims 10 – 11 only, none of these cited references shows or suggests the above-mentioned technical feature of the present invention.

Donnelly et al. only discloses the oxygen plasma treatment which serves a completely different function from that of the annealing treatment of the present invention. In Donnelly et al. the oxygen plasma treatment is performed to remove the above-mentioned organic substance and thus the reduction treatment in Donnelly et al. is carried out utilizing organic gas such as, for example, hexafluoro-acetyl-acetone or the like.

If organic gas is utilized for the instant invention, as explained on page 9, lines 26-29 of the specification, a separate problem would arise in that contamination, caused by re-deposition of carbon generated by dissolution of the organic gas, will appear. In the present invention, by solving the above-mentioned problem, a cleaner process for eliminating oxides of copper can be realized.

Further, regarding claims 6 and 7, the Examiner stated that it would be obvious to a person skilled in the art to perform an annealing treatment in a sputtering chamber just before the sputtering operation to form a barrier film, since a conventional sputtering apparatus is usually provided with a gas introducing mechanism and a heater element.

However, it is respectfully submitted that when an oxygen plasma treatment would be introduced into the conventional sputtering apparatus, a surface of a metal (such as Ti, Ta or the like) used for a target, would be highly oxidized so as to form titanium oxide film or tantalum oxide film on the surface of the target. When the sputtering treatment would be carried out thereafter, the titanium oxide film or tantalum oxide film, each having an extremely low level of conductivity, would be deposited on a surface of a device causing the generation of further dusts and making this process impractical.

In conclusion, the present invention is a sophisticated invention based upon actual experimental results, namely, that the copper oxide film formed on a surface of copper metal can be effectively reduced by utilizing an annealing treatment under a vacuum condition or low oxygen partial pressure. Thus, the objects and functions, as well as advantages, of the present invention are completely different from the oxygen plasma treatment disclosed in the cited references.

Applicant mailed an Information Disclosure Statement (IDS) on June 17, 2002, but did not receive a Form PTO-1449, from such IDS, properly signed and initialed by the Examiner with the Office Actions to which this amendment is responsive. The Examiner is respectfully requested to return a copy of such Form PTO-1449, with the next Office Action.

Attached hereto is a marked-up version of the changes made to the specification and claim 2 by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

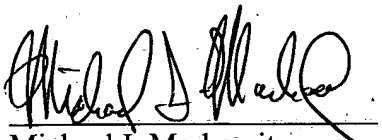
CLOSING

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claim 2 is in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,



Michael I. Markowitz
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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph on page 8, lines 3-4, has been rewritten as follows:

The surface of the copper interconnect layer 1, [not being] is covered by the SIN layer 2, and thus is not exposed.

IN THE CLAIMS

Claims 2 and 3 have been rewritten as follows:

2. (Once Amended) A method for forming a via hole of a semiconductor device comprising:

a step of forming a first step via hole in a laminated structure formed by a copper layer, an etching-stop layer formed on a surface of said copper layer, and an insulation layer formed on a surface of said etching-stop layer, thereby a bottom of said first step via hole is stopped at said etching-stop layer;

a step of forming a second step via hole continuous with said first step via hole in said etching-stop layer, thereby a bottom of said second step via hole reaching at [a] said surface of said [interconnect] copper layer;

a step of cleaning said second step via [hole;] hole,said step of cleaning including an annealing process for said via hole; and

a step, after said cleaning, of forming a barrier film on said first and second step via holes, by [sputtering.]

3. (Once Amended) A method for forming a via hole of a semiconductor device according to claim 2, wherein said [step of cleaning said via hole comprises a step for] annealing process for said via hole is performed at a low oxygen partial pressure.